Major Benefits of IEEE 1149.7

While the electronics industry continues to produce the next generation of integrated circuits to meet the ever growing consumer demand for increased performance, reduced power consumption and lower cost, new industry-wide challenges are arising that address how to debug and test these highly complex devices. Each successive new IC generation integrates more logic and functionality into a smaller physical size. It is becoming increasingly more difficult to balance the practical needs of accessing the internal test logic and debug circuitry while still meeting the strict functional performance and cost requirements.

IEEE Standard 1149.1, commonly referred to as JTAG (Joint Test Action Group), provides a convenient and standardized method to communicate with embedded devices. The IEEE 1149.1 standard is widely used in boundary-scan testing tools to detect structural manufacturing defects in the solder interconnects that may occur during board assembly and as a platform for developing and debugging embedded software and firmware during system bring-up and board verification.

While JTAG has been in use for over 20 years, and will probably continue to be used far into the foreseeable future, the recently released standard IEEE 1149.7 (Standard for Reduced-pin and Enhanced-functionality Test Access Port and Boundary Scan Architecture) has been created to improve upon it and extend its capabilities. The goal was not to replace IEEE standard 1149.1 but to create a complementary standard that addresses the recent changes in the integrated circuit technology and topology. The new standard builds on the existing one in order to implement additional functionality and maximize debug performance while simultaneously maintaining backwards compatibility.

The new IEEE 1149.7 standard (cJTAG or Compact JTAG) provides several major benefits to both board designers and embedded engineers.

Summary of Major New Features

- Reduced pin count
- Star topology
- Individual device addressing
- Chip level bypass
- Additional power management features

Summary of Major Benefits

- Simplified connections between devices
- Improved support for devices with multiple cores
- Increased debug performance

Reduced Pin Count

One of cJTAG's most significant extensions to the existing IEEE standard 1149.1 is the addition of a 2-pin TAP interface capability where data in transferred using only the TMS and TCK pins. The TDI and TDO

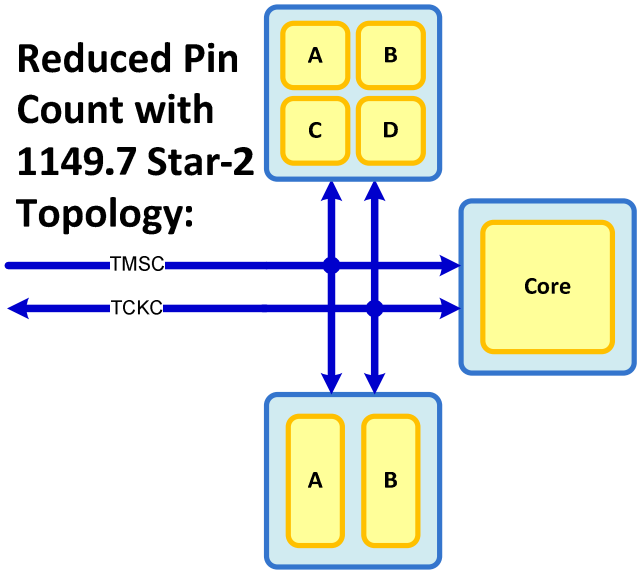
signals may be removed while still allowing access to the previous functionality or the new advanced scan protocols. This is significant because most modern embedded systems integrate multiple ICs and often have severe size constraints. Dedicated pins for bringing out chip debug and test functionality is desirable during board development and production but raises the overall cost of the devices. It is costly both in terms of money and real estate to dedicate special pins for bringing debug and test signals out, especially as device vendors are pressured to make the IC packages smaller.

By only requiring a two-pin interface for operation instead of the four pins required in IEEE 1149.1, the 1149.7 standard allows more test and debug functionality to reside on a reduced number of external pins. Fewer pins, nets and discrete components like pull-up resistors also makes routing and trace layout much easier, particularly in applications like stacked-die devices and multi-chip modules where various components are vertically stacked. Reducing the number of pins needed for test also lowers the overall packaging cost, frees up pins for implementing additional features and functionality and helps device and board designers meet their form factor and cost constraints.

Star Topology

The star topology is one of several enhancements in the IEEE 1149.7 standard for gracefully handling arrays of identical devices and devices with multiple cores. These can be boards with 32 DSPs or multi-core CPU or Systems-on-Chip (SoC) with separate physical processors, stacked die configurations or multichip System-in-Package (SiP) modules with several distinct peripherals within the same physical package.

The introduction of a star topology in the IEEE 1149.7 standard complements the reduced pin count. Designers working with stacked-die devices, multi-chip modules and plug-in cards will favor the star topology and 2-pin interface because it simplifies the physical connections between devices.

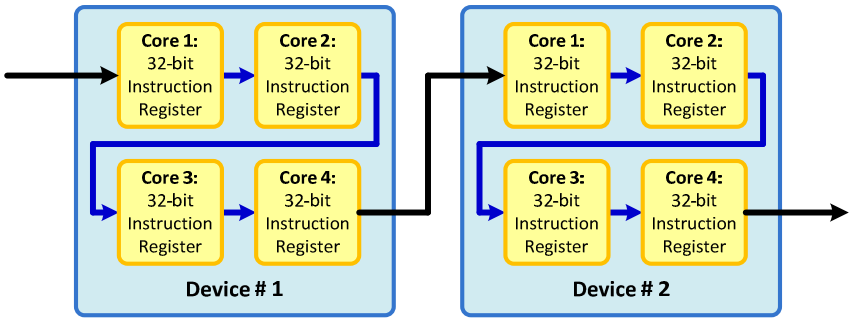


Chip Level Bypass and Individual Device Addressing

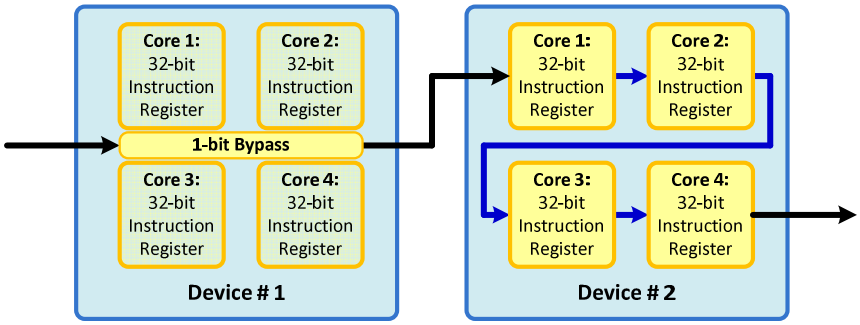
Not only does the IEEE 1149.7 standard better support devices with multiple cores and internal peripherals, it also does so more efficiently. The serial design architecture of the existing JTAG standard made it very difficult to communicate exclusively with one specific device in the scan chain due to interactions with other devices in the chain, particularly when multiple devices or cores are combined into one physical package. The standard provides a method to address and access specific devices in the scan chain individually, without having to shift bits through the entire instruction register length of the full scan chain.

A chip level bypass mechanism has been implemented to reduce the overall scan chain length by putting unused devices in a 1-bit chip bypass mode. Utilizing this feature can make very long scan chains dramatically shorter and improve the overall scan efficiency and throughput.

Scan Chain Without Chip Level Bypass:



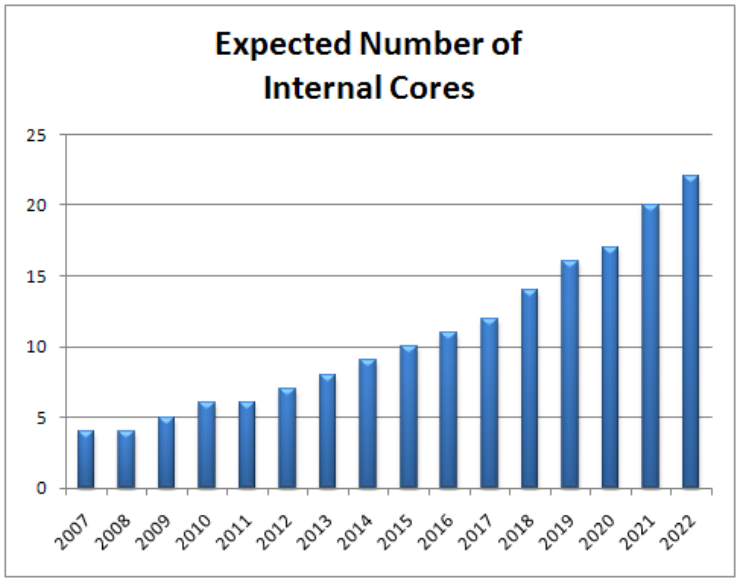
Equivalent Scan Chain With IEEE 1149.7 Chip Level Bypass:



The individual addressing and chip level bypass capability provided by the new standard allows the host controller to communicate with only the intended device. This allows for increased performance and extends the capability of the current standard by enabling more advanced debug and instrumentation logic to be designed into the individual chips. The new standard provides a common method to communicate with the enhanced functionality and the host can now address multiple internal modules through the same 2 or 4-pin TAP interface.

The ability to quickly access a specific device in a system with multiple devices also directly improves the ease of debugging a complicated system. This is extremely important because the International

Technology Roadmap for Semiconductors (ITRS) currently expects that the number of internal cores will roughly double with each new processor generation[i].



Power Management

One limitation of the IEEE 1149.1 (JTAG) standard is that devices only have a single power state while being tested. A device has to be either completely on or completely off while the boundary-scan tests are executing.

The IEEE 1149.7 standard provides a standardized interface with four selectable power modes to control the device power. This capability to control the power consumption of the debug logic or individually adjust the power state of multiple cores in a device will make boundary-scan testing much easier in many board designs.

About Corelis

Corelis, Inc., a subsidiary of EWA Technologies, Inc., offers the industry's broadest line of boundary-scan software and hardware products that combine exceptional ease-of-use with advanced technical innovation and unmatched customer service. Corelis' ScanExpress Boundary-Scan systems are used for interconnect testing and In-System Programming (ISP) of Flash memories, CPLDs, and FPGAs. Systems include a complete range of IEEE-1149.1 compatible boundary-scan controllers for PCI, PC-Card, Ethernet, USB 2.0, cPCI/cPXI, and VXI host interfaces. Corelis also provides custom test engineering services, including test procedure development and integration. For more information about Corelis, please visit **www.corelis.com**.

[i] THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: 2007