

# Boundary-Scan Parallel Test and Programming Cuts Costs and Simplifies Production of High-Volume Telephony Products



Figure 1. Zultys VoIP Equipment.



*"...Manufacturers also save money—as much as \$5,000 to \$10,000 per project—by generating and re-using the same test vectors for both design and manufacturing."*

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The market for voice over IP (VoIP) products is one of the fastest growing and fastest evolving markets in the high-tech world. Enterprise level VoIP is expected to grow 20% annually through 2009, according to The Insight Research Group. To stay on the leading edge, companies like Zultys Technologies must emphasize short time-to-market, lowered costs, and superior quality.

With demand growing so fast, IP telephony products like those from Zultys are characterized by an all new cost model that requires maximum yield in manufacturing. In addition, the products call for more complex and powerful components that must be packed into ever smaller circuit boards. One of the ways these companies can deliver on these promises is through the use of the latest manufacturing and test technologies. Zultys sees these technologies as a competitive edge in manufacturing its VoIP telephones for the enterprise market.

Fortunately, more and more of the new intelligent processors and communication electronics are designed to include boundary-scan chains. Boundary-scan testing of multiple circuit boards in parallel is one way to cut both time and costs out of the test cycles of product manufacturing. A single operator can test multiple boards simultaneously from a single PC. With these new boundary-scan (JTAG) tools, it takes the same amount of time to test 4 boards or 1,000.

### **Only Boundary-Scan is a Natural for Parallel, Electronic Test and Programming**

The concept of testing product boards simultaneously matches perfectly with the electronic nature of boundary-scan. No other testing technology can accomplish the same thing. JTAG (Joint Test Action Group IEEE standard), which provides test access to integrated circuits via a four- or

five-pin external interface, enables concurrent (gang) testing and in-system programming of CPLDs and Flash devices for multiple boards using a single PC and a single operator.

The latest boundary-scan hardware autonomously performs concurrent testing and programming of multiple units without software intervention. The Test Access Ports (TAPs) on the remote test pod have a dedicated pin on the JTAG interface connector that can detect the presence of the target board. The software monitors the state of this signal to detect both the presence of the target device as well as the proper insertion of the test cable.

The hardware applies simultaneous test vectors and In-System Programming (ISP) patterns to each board, as well as individual, simultaneous verification. Any failure of one board will be logged, but doesn't prohibit the continuation of testing on all the other units under test (UUT).

A key requirement for Zultys was to reduce test time to keep up with a "push-line" assembly process. The push-line uses a conveyor belt to move product down the assembly line through a series of stations. Once all the components are added and wired, the product moves to JTAG stations near the end of the line. The company chose the ScanExpress system from Corelis, Inc. Zultys has two JTAG programming and test stations, each with four phones in parallel. In addition to the boot Flash which is common to every unit, each phone has unique information programmed into its Flash.

A Visual Basic application takes the barcode input for each UUT and creates a .hex file for each UUT.

"My JTAG tools allow me to perform Infrastructure, Interconnect, and Boot Flash programming of all four UUTs in parallel and then separately apply the unique data files to the appropriate UUTs," said Bob Shoemaker, Manager of Manufacturing Engineering at Zultys. "This is something we couldn't have done before."

Of course, besides the electronic capability to perform the tests and programming on large numbers in parallel, manufacturers need to accommodate the hardware and cabling on their floor in a feasible physical setup as well. The latest boundary-scan hardware and software architectures are designed for up to 30 feet of extended distance from the test PC to the TAP pod, with no need for TAP extenders. Also, the system applies automatic signal delay compensation for long cable runs from the TAP to the units under test.

### The Flexibility To Match A Fast-Changing Market

It's not unusual for manufacturers to find that markets offering significant growth opportunities typically involve the most complex products, since that's where the manufacturer can add the most value for their customers. At the same time, those types of products often need to quickly change design to accommodate new components and firmware, so flexibility on the manufacturing floor is paramount.

The single PC-based controller means changing only one set of test and programming files when changes are implemented. Engineers and technicians can create the files, try them on a single unit, then apply the same test in parallel to N units. Manufacturers also save money – as much as \$5,000 to \$10,000 per project – by generating and re-using the same test vectors for both design and manufacturing.



**Figure 2.** The JTAG software can match unique software to targeted boards and download common software code all in one test and programming cycle.

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### More Automation and a Simple Interface Benefit Experienced and Novice Users

The new generation of automatic boundary-scan test pattern generation tools provide automation that makes boundary-scan extremely easy to use. This feature can be especially valuable when products are manufactured overseas where labor costs are low, but test operators may be less familiar with the English language.

"Labor is relatively inexpensive in China, so when you look at the cost of product testing, ease-of-use is more valued than actual test time," says Shoemaker.

Both experienced and novice users can create boundary-scan test vectors in a fraction of the time it takes to develop these test vectors using legacy test-pattern generators. The tools automatically generate test patterns that facilitate the pin-level fault detection and isolation of all boundary-scan testable nets on a printed circuit board (PCB). They also create test vectors to detect faults on the pins of non-scanable components, such as clusters and memories that are surrounded by scanable devices.

A single Graphical User Interface (GUI) provides the integrated development environment (IDE) for users to generate boundary-scan tests from scratch, produce test coverage reports, and invoke the controller software to execute created tests. The user starts with the basic board design files, adds supplemental information, generates test vectors, creates test coverage reports, and executes the tests by using descriptive icons located on a shortcuts bar.

"All the test vectors and programming files that are created with the ScanExpress system are applied without any change to test and program our products in parallel," added Shoemaker.

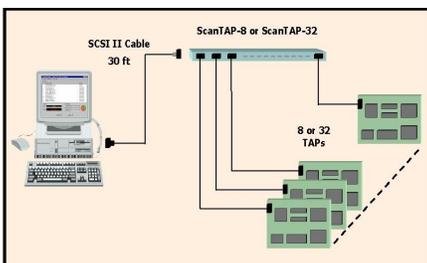
Software in the test controller can execute boundary-scan tests and various ISP files from third party applications using DLLs or a command line interface. Drivers include the popular National Instruments LabWindows/CVI, LabView, and Agilent VEE test environments.

### Controller Scan Rate Is Independent of Host Computer Speed

The boundary-scan controller card is the key element of the system. The most advanced PCI, USB, LAN, or CPXI controllers are designed to include several performance enhancing functional sections aimed at increasing test vector and in-system programming throughput. The combination of these functional elements results in a very high data scanning rate, which is completely decoupled from the bus and the speed of the host computer.

The system-wide test clock (TCK) rate for all TAP ports is programmable under software control. On-board Phase-Locked-Loop (PLL) generation circuitry can provide a wide range of TCK frequencies. Technicians can select the desired TCK rate from a range of values up to 80 MHz at resolution increments of less than 2%. Should an external TCK timing reference be required for synchronization, or a user-unique frequency, an external SMB connector can be used.

A key criterion for the boundary-scan system is that, no matter what clock rate is selected, it should be able to scan at that TCK continuously. This gives the hardware architecture the ability to supply the data and pattern comparisons without having dead states or wait states. Some hardware can scan at high TCK, but only at peak intervals, and then must wait while the hardware scans more data out or while patterns are compared.



**Figure 3.** ScanTAP-32 with 32 Concurrent JTAG Ports

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### A Modular, Expandable System Can Expand to Match Mass Volumes Quickly and at Low-Cost

Manufacturers should also look for testing hardware that is modular and easy to expand. That enables test technicians to easily connect new hub devices or multi-port TAP pods to expand from a few boards to hundreds or even thousands.

As **Figure 3** shows, the most simple test setup is to connect the test controller to a PC through a PCI, USB, LAN, or CPXI interface, then to multiport TAP pods to accommodate the UUT. TAP pods are available in four-, eight- or 32-port configurations. **Figure 4** depicts a multi-port pod from Corelis with 32 concurrent JTAG ports. From there, additional hardware choices fan the connection out to accommodate more and more units at once.

Users can also connect first to a hub device that can connect to as many as 16 TAP pods. To further expand the system, a second tier of 16-port hubs can be added to the expansion ports of the primary hub. This configuration fans out the controller to as many as 256 (16×16) TAP pods. Since each pod can drive up to 32 TAPs, this simple building-block test system can concurrently scan up to 8,192 TAPs in total.

The scan patterns generated by the controller are then distributed to the target system either directly through the TAP pods or through a hub. The TAP pods can apply test vectors, ISP patterns, or both to target boards with a variety of JTAG chain topologies.

If the board under test consists of groups that include multiple devices, each with their own respective TAP, then the TAP pods allow for test vectors to be applied to each of the target TAPs individually, one TAP at a time, or jointly to all of the TAPs.

#### About Zultys Technologies

Incorporated in 2001, Zultys Technologies has its headquarters in Sunnyvale, California. Zultys designs and manufactures products that converge telecommunications and data communications for businesses. Zultys develops its hardware and software specifically to create products that deliver completely integrated solutions, allowing for ease of deployment, management, and use. These products support multiple languages and are based on open standards to ensure interoperability in a network. After installation, productivity increases and operating costs decrease. Zultys sells its products worldwide and has distribution today in 115 countries. For more information on Zultys or its products, access: <http://www.zultys.com>.

#### About Corelis

Corelis, Inc., a subsidiary of Electronic Warfare Associates, Inc., offers bus analysis tools, embedded test tools, and the industry's broadest line of JTAG/boundary-scan software and hardware products combining exceptional ease-of-use with advanced technical innovation and unmatched customer service. Corelis' development and test tools are used by companies such as Agilent, Dell, IBM, Intel, Microsoft, Lockheed Martin, Rockwell Collins, Hewlett-Packard, Motorola, Qualcomm, Nokia, Panasonic, TI, Ford, Broadcom, Ericsson, and many others. Corelis products are found globally in every industry developing or manufacturing electronic products.



**Figure 4.** ScanTAP-32 with 32 Concurrent JTAG Ports

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